

915GV-M6

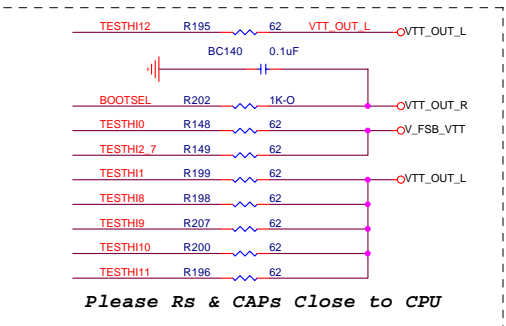
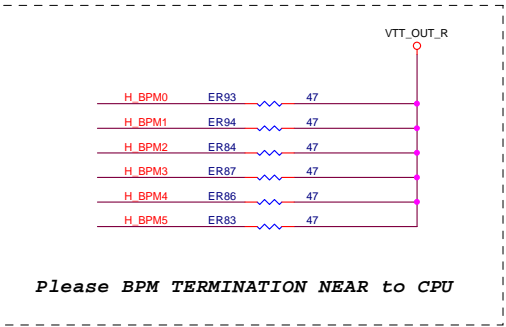
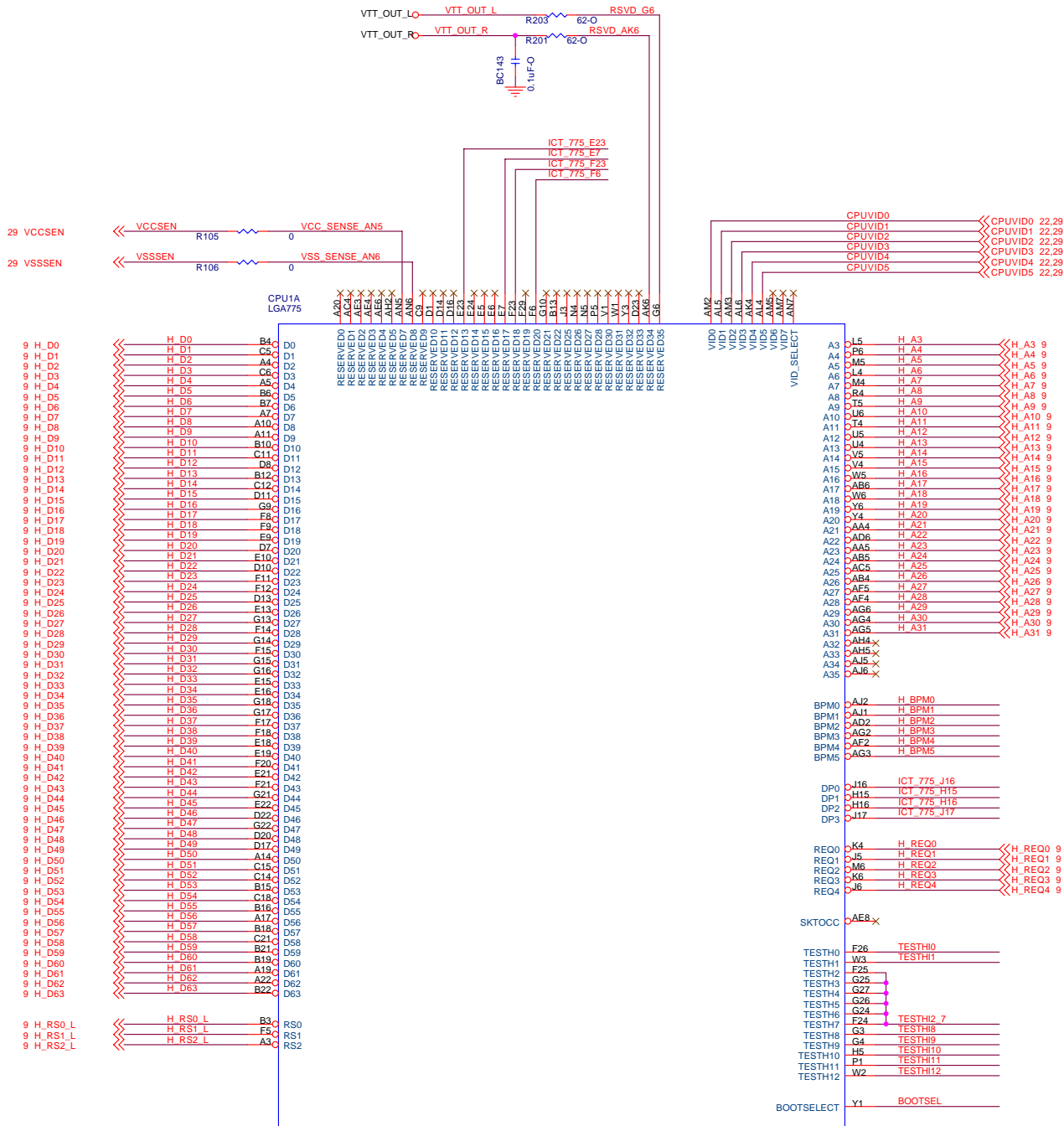
Rev: 1.0

Page Title of Schematic :

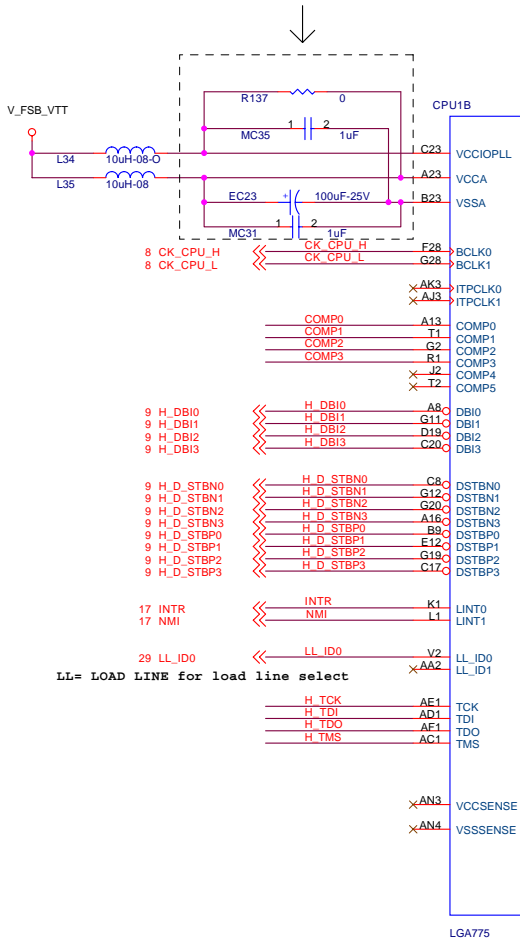
Schematics Version History Table :

Circuit Ver.	PCB Ver.	Total Page	Modified Page(s)	Date
A	A	34		10/26/' 04
1.0	1.0	34		12/21/' 04

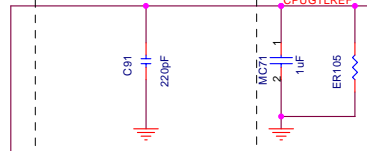
Title	Page	Title	Page
Cover Sheet	1		
System Block Diagram	2		
P4 LGA775P Part A	3		
P4 LGA775P Part B	4		
P4 LGA775P Part C	5		
P4 LGA775P Part D	6		
P4 LGA775P Part E	7		
Clock Generator(CK410)	8		
I-GSD(MCH)Part A & E & F	9		
I-GSD(MCH)Part D	10		
I-GSD(MCH)Part B & C	11		
I-GSD(MCH)Part G	12		
DDIMM 1&2 (DDR SDRAMs)	13		
DDIMM 3&4 (DDR SDRAMs)	14		
DDR & V_FSB_VTT Power	15		
PCI EXPRESS 16-PORT	16		
ICH6 Part A & D (SATA-CONNECTOR)	17		
ICH6 Part B & C (RTC)	18		
ICH6 Part E & F (POWER & GND)	19		
IDE1 Connector	20		
USB/FWH	21		
LPC_FDD/KB/M	22		
I/O Ports	23		
H/W Monitor	24		
AC97 Codec	25		
Audio Interface	26		
ATX Power & Front Panel	27		
LAN	28		
Vcore DC-DC	29		
MIS DC-DC(DUAL & VDDQ)	30		
PCI Slot 1&2	31		
PCI Slot 3	32		
Back I/O	33		
Schematic Change History	34		



Place componets as close as possible to Processor socket
trace width to cap must be no smaller than 12 Mils

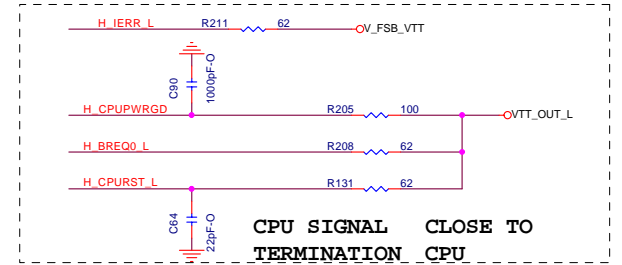


Close CPU H1 pin



$$GTLREF = 0.67 * VTT = 0.8V$$

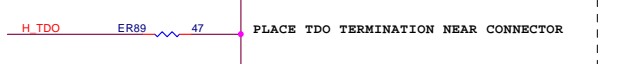
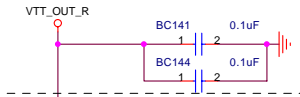
GTLREF GENERATION CIRCUITS



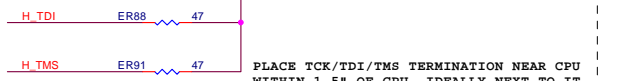
CPU SIGNAL CLOSE TO TERMINATION CPU



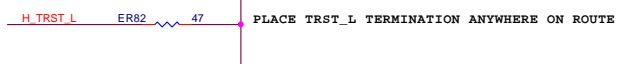
BSEL resistors can be removed IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED



PLACE TDO TERMINATION NEAR CONNECTOR

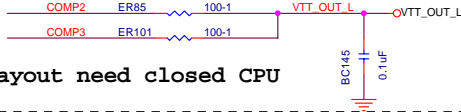


PLACE TCK/TDI/TMS TERMINATION NEAR CPU WITHIN 1.5" OF CPU, IDEALLY NEXT TO IT.

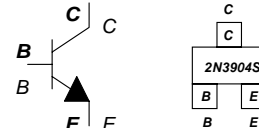
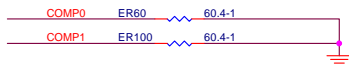


PLACE TRST_L TERMINATION ANYWHERE ON ROUTE

Layout need closed CPU




Place outside Socket Cavity



Title			
P4 LGA775P Part B			
Size	Document Number	Rev	
Custom	915GV-M6	1.0	
Date:	Tuesday, December 21, 2004	Sheet	4 of 34



CPU1C
LGA775



Elitegroup Computer Systems

Title

P4 LGA775P Part C

Size

Custom

Document Number

915GV-M6

Date:

Tuesday, December 21, 2004

Sheet

5

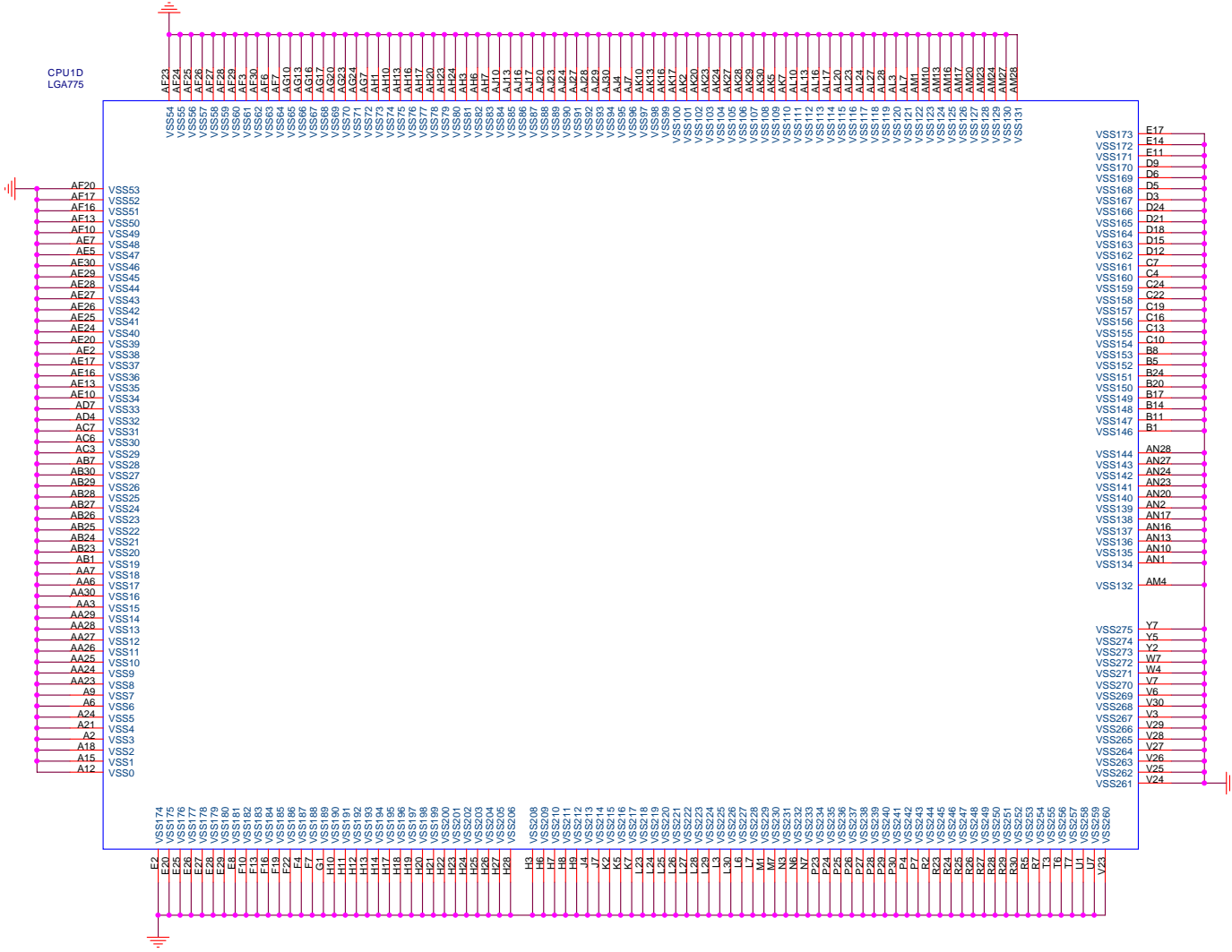
of

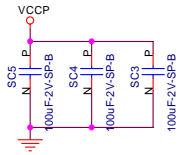
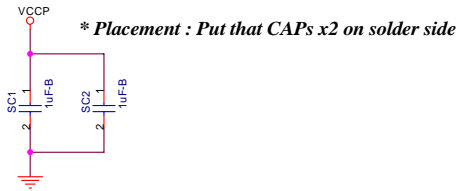
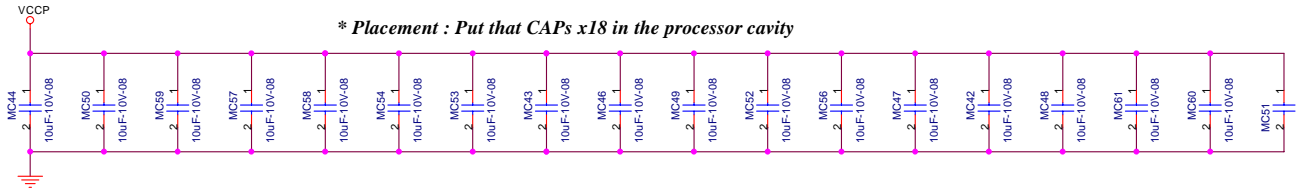
34

Rev

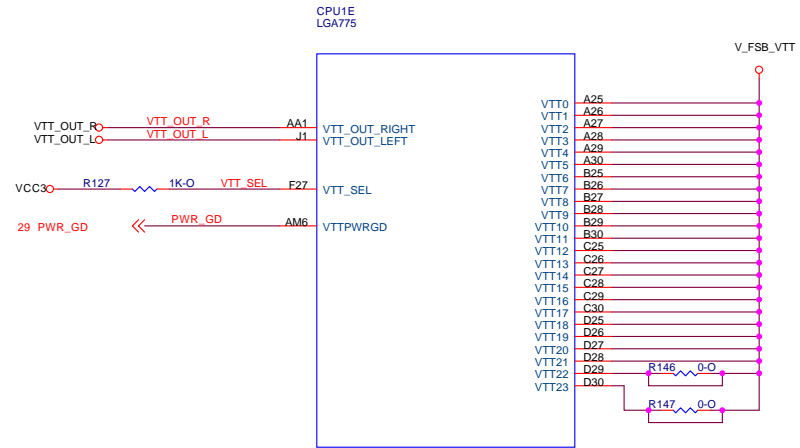
1.0

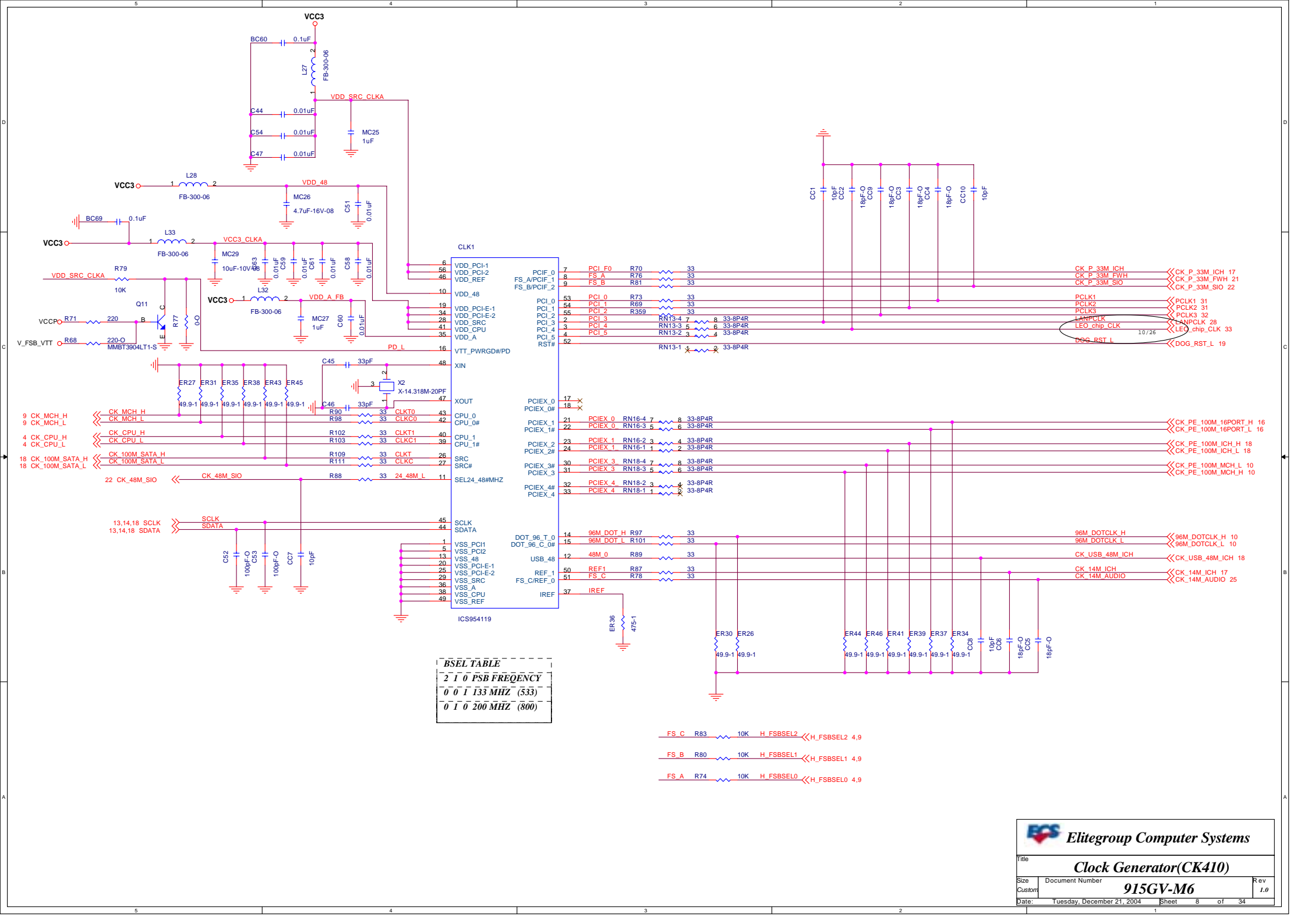
CPU1D
LGA775



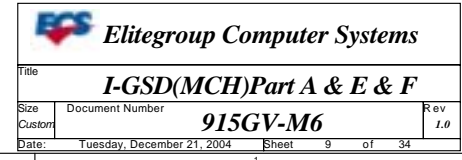


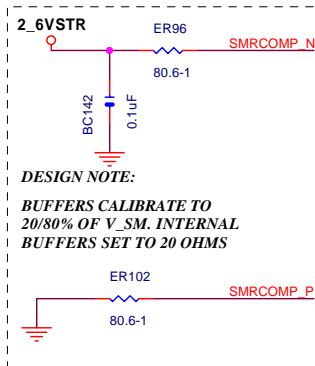
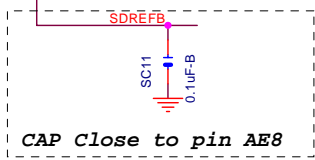
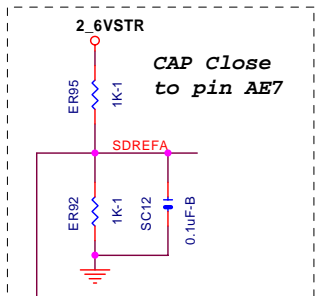
VTT_SEL=0 for the Tejas processor





BSEL TABLE									
2	1	0	PSB	FREQUENCY					
0	0	1	133 MHZ	(533)					
0	1	0	200 MHZ	(800)					





DESIGN NOTE:
BUFFERS CALIBRATE TO
20/80% OF V_{SM}. INTERNAL
BUFFERS SET TO 20 OHMS

MD A63	T35	SDQ A63	MD A62	T33	SDQ A62	MD A61	W35	SDQ A61	MD A59	W35	SDQ A60	MD A58	R34	SDQ A59	MD A57	V23	SDQ A58	MD A56	V24	SDQ A57	MD A55	V24	SDQ A56	MD A54	V23	SDQ A55	MD A53	V23	SDQ A54	MD A52	V23	SDQ A53	MD A51	V23	SDQ A52	MD A50	V23	SDQ A51	MD A49	AE34	SDQ A50	MD A48	AE35	SDQ A49	MD A47	AE35	SDQ A48	MD A46	AE35	SDQ A47	MD A45	AE35	SDQ A46	MD A44	AE35	SDQ A45	MD A43	AE34	SDQ A44	MD A42	AG32	SDQ A43	MD A41	AH35	SDQ A42	MD A40	AH34	SDQ A41	MD A39	AG34	SDQ A40	MD A38	AG35	SDQ A39	MD A37	AG35	SDQ A38	MD A36	AL27	SDQ A37	MD A35	AN30	SDQ A36	MD A34	AN30	SDQ A35	MD A33	AN30	SDQ A34	MD A32	AH27	SDQ A33	MD A31	AH30	SDQ A32	MD A30	AE19	SDQ A31	MD A29	AE17	SDQ A30	MD A28	AE19	SDQ A29	MD A27	AE19	SDQ A28	MD A26	AD17	SDQ A27	MD A25	AD17	SDQ A26	MD A24	AH16	SDQ A25	MD A23	AH16	SDQ A24	MD A22	AE17	SDQ A23	MD A21	AE17	SDQ A22	MD A20	AE17	SDQ A21	MD A19	AE19	SDQ A20	MD A18	AE19	SDQ A19	MD A17	AE19	SDQ A18	MD A16	AE19	SDQ A17	MD A15	AE19	SDQ A16	MD A14	AE19	SDQ A15	MD A13	AE19	SDQ A14	MD A12	AE19	SDQ A13	MD A11	AE19	SDQ A12	MD A10	AE19	SDQ A11	MD A9	AE19	SDQ A10	MD A8	AE19	SDQ A9	MD A7	AE19	SDQ A8	MD A6	AE19	SDQ A7	MD A5	AE19	SDQ A6	MD A4	AE19	SDQ A5	MD A3	AE19	SDQ A4	MD A2	AE19	SDQ A3	MD A1	AE19	SDQ A2	MD A0	AE19	SDQ A1	MD A0	AE19	SDQ A0
--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	--------	------	---------	-------	------	---------	-------	------	--------	-------	------	--------	-------	------	--------	-------	------	--------	-------	------	--------	-------	------	--------	-------	------	--------	-------	------	--------	-------	------	--------	-------	------	--------

DDR1 Channel A

REV=1.0

GMCHB
Grantsdale DDR1 MCH_7

MD B63	V28	SDQ B63	MD B62	W28	SDQ B62	MD B61	W28	SDQ B61	MD B60	W28	SDQ B60	MD B59	W28	SDQ B59	MD B58	W28	SDQ B58	MD B57	W28	SDQ B57	MD B56	W28	SDQ B56	MD B55	W28	SDQ B55	MD B54	W28	SDQ B54	MD B53	W28	SDQ B53	MD B52	W28	SDQ B52	MD B51	W28	SDQ B51	MD B50	W28	SDQ B50	MD B49	W28	SDQ B49	MD B48	W28	SDQ B48	MD B47	W28	SDQ B47	MD B46	W28	SDQ B46	MD B45	W28	SDQ B45	MD B44	W28	SDQ B44	MD B43	W28	SDQ B43	MD B42	W28	SDQ B42	MD B41	W28	SDQ B41	MD B40	W28	SDQ B40	MD B39	W28	SDQ B39	MD B38	W28	SDQ B38	MD B37	W28	SDQ B37	MD B36	W28	SDQ B36	MD B35	W28	SDQ B35	MD B34	W28	SDQ B34	MD B33	W28	SDQ B33	MD B32	W28	SDQ B32	MD B31	W28	SDQ B31	MD B30	W28	SDQ B30	MD B29	W28	SDQ B29	MD B28	W28	SDQ B28	MD B27	W28	SDQ B27	MD B26	W28	SDQ B26	MD B25	W28	SDQ B25	MD B24	W28	SDQ B24	MD B23	W28	SDQ B23	MD B22	W28	SDQ B22	MD B21	W28	SDQ B21	MD B20	W28	SDQ B20	MD B19	W28	SDQ B19	MD B18	W28	SDQ B18	MD B17	W28	SDQ B17	MD B16	W28	SDQ B16	MD B15	W28	SDQ B15	MD B14	W28	SDQ B14	MD B13	W28	SDQ B13	MD B12	W28	SDQ B12	MD B11	W28	SDQ B11	MD B10	W28	SDQ B10	MD B9	W28	SDQ B9	MD B8	W28	SDQ B8	MD B7	W28	SDQ B7	MD B6	W28	SDQ B6	MD B5	W28	SDQ B5	MD B4	W28	SDQ B4	MD B3	W28	SDQ B3	MD B2	W28	SDQ B2	MD B1	W28	SDQ B1	MD B0	W28	SDQ B0	MD B0	W28	SDQ B0
--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	--------	-----	---------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------	-------	-----	--------

DDR2 Channel B

REV=1.0

GMCHC
Grantsdale DDR1 MCH_7

- 13 MD_A[0..63] << MD_A[0..63]
- 14 MD_B[0..63] << MD_B[0..63]
- 13 DQS_L_A[0..7] << DQS_L_A[0..7]
- 14 DQS_L_B[0..7] << DQS_L_B[0..7]
- 13 MPD_A[0..7] << MPD_A[0..7]
- 14 MPD_B[0..7] << MPD_B[0..7]
- 13 MAAA_[0..13] << MAAA_[0..13]
- 14 MAAB_[0..13] << MAAB_[0..13]

- 13 CSA_L[0..1] << CSA_L[0..1]
- 14 CSB_L[0..1] << CSB_L[0..1]
- 13 CKEA_[0..1] << CKEA_[0..1]
- 14 CKEB_[0..1] << CKEB_[0..1]
- 13 DCLKA_L[0..2] << DCLKA_L[0..2]
- 14 DCLKA_H[0..2] << DCLKA_H[0..2]

- 14 DCLKB_L[0..2] << DCLKB_L[0..2]
- 14 DCLKB_H[0..2] << DCLKB_H[0..2]
- SWE_L_A << SWE_L_A 13
- SCAS_L_A << SCAS_L_A 13
- SWE_L_B << SWE_L_B 14
- SCAS_L_B << SCAS_L_B 14
- SBSA_0 << SBSA_0 13
- SBSA_1 << SBSA_1 13
- SBSB_0 << SBSB_0 14
- SBSB_1 << SBSB_1 14

Elitegroup Computer Systems

I-GSD(MCH)Part B & C

Title

Size B Document Number 915GV-M6 Rev 1.0

Date: Tuesday, December 21, 2004 Sheet 11 of 34


Grantsdale DDR1 MCH_7

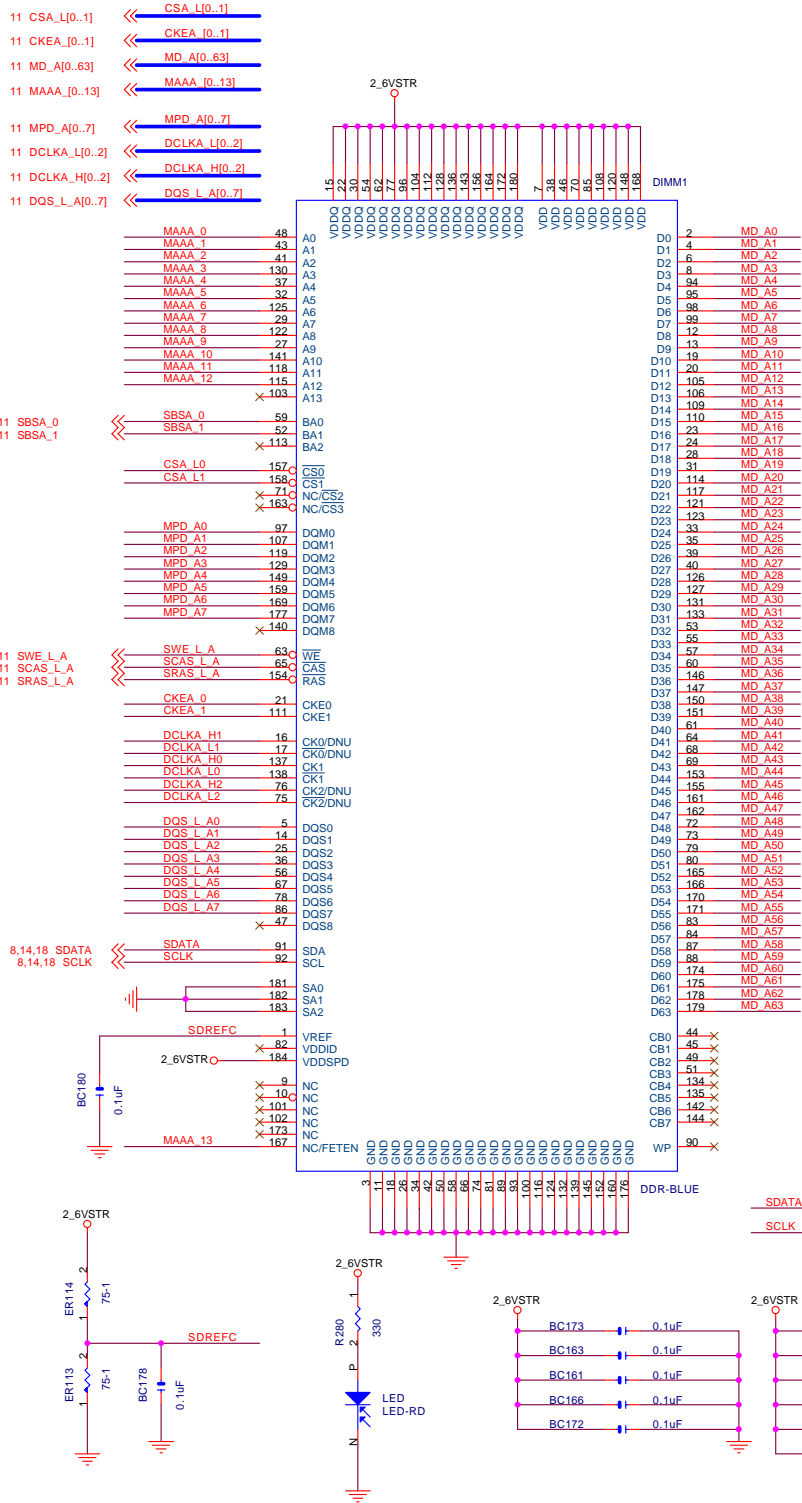
GMCHG

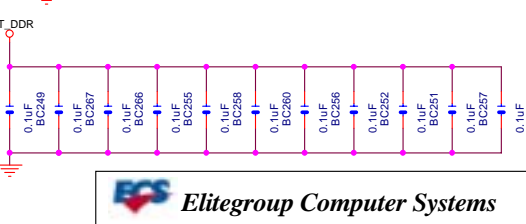
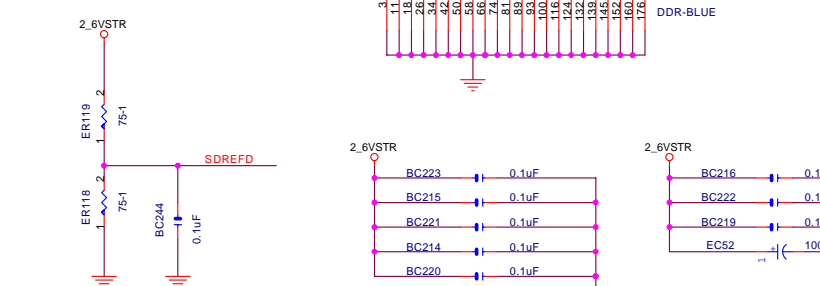
RSV

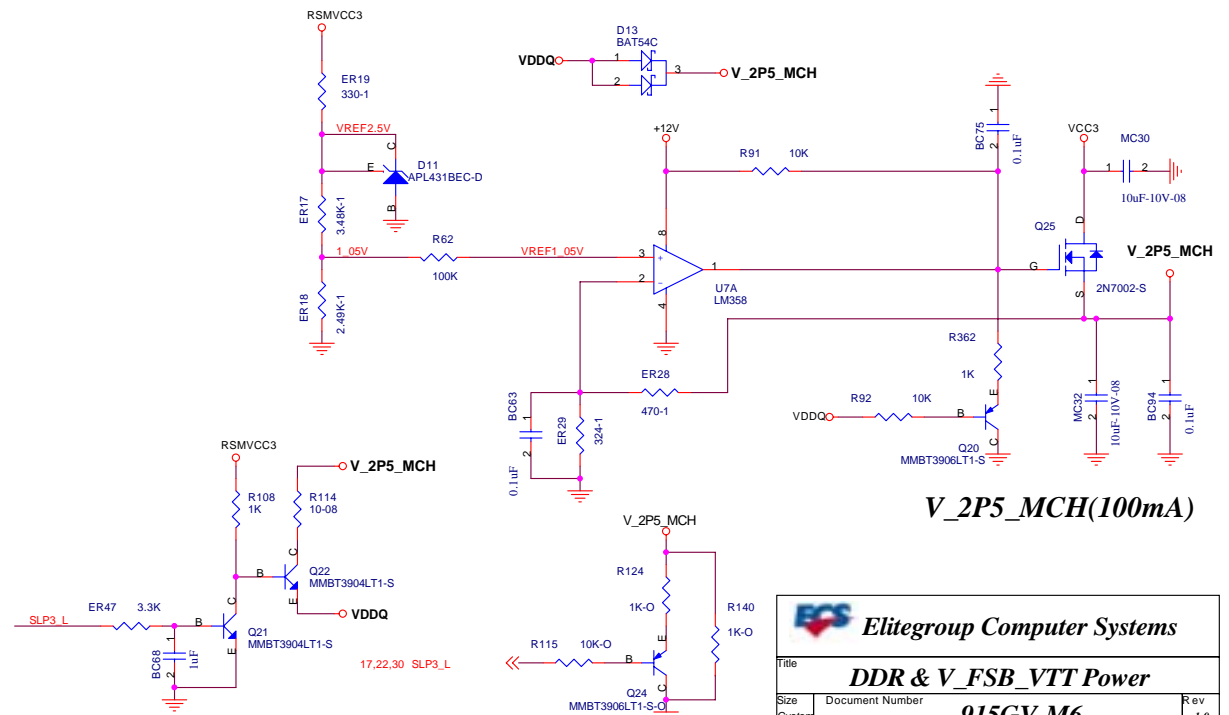
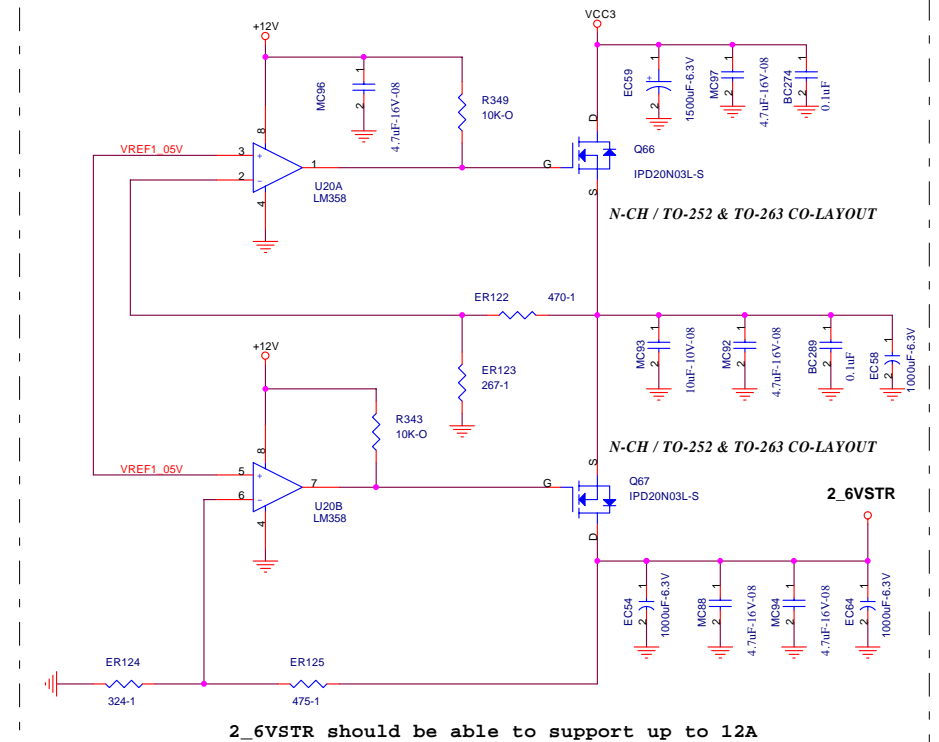
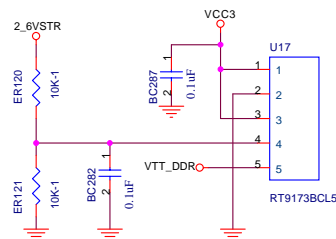
GND

REV=1.0

 Elitegroup Computer Systems	
Title	
Schematic Change History	
Size	Document Number
Custom	915GV-M6
Date:	Tuesday, December 21, 2004
Sheet	12 of 34





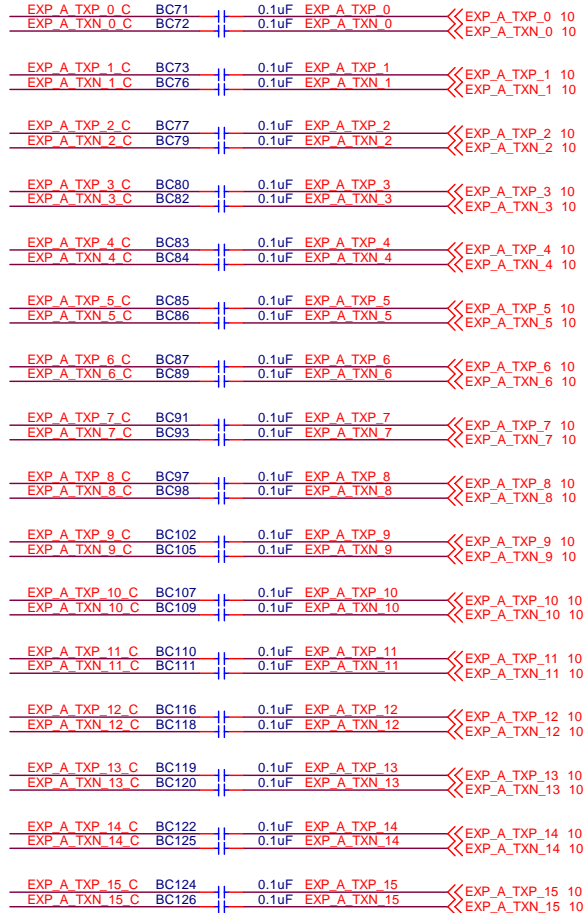
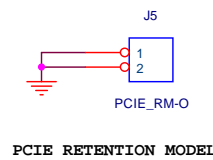
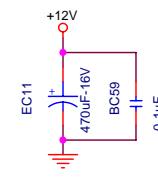
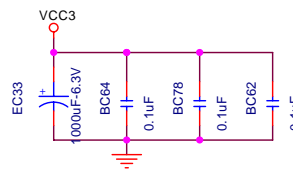
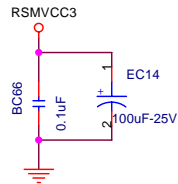
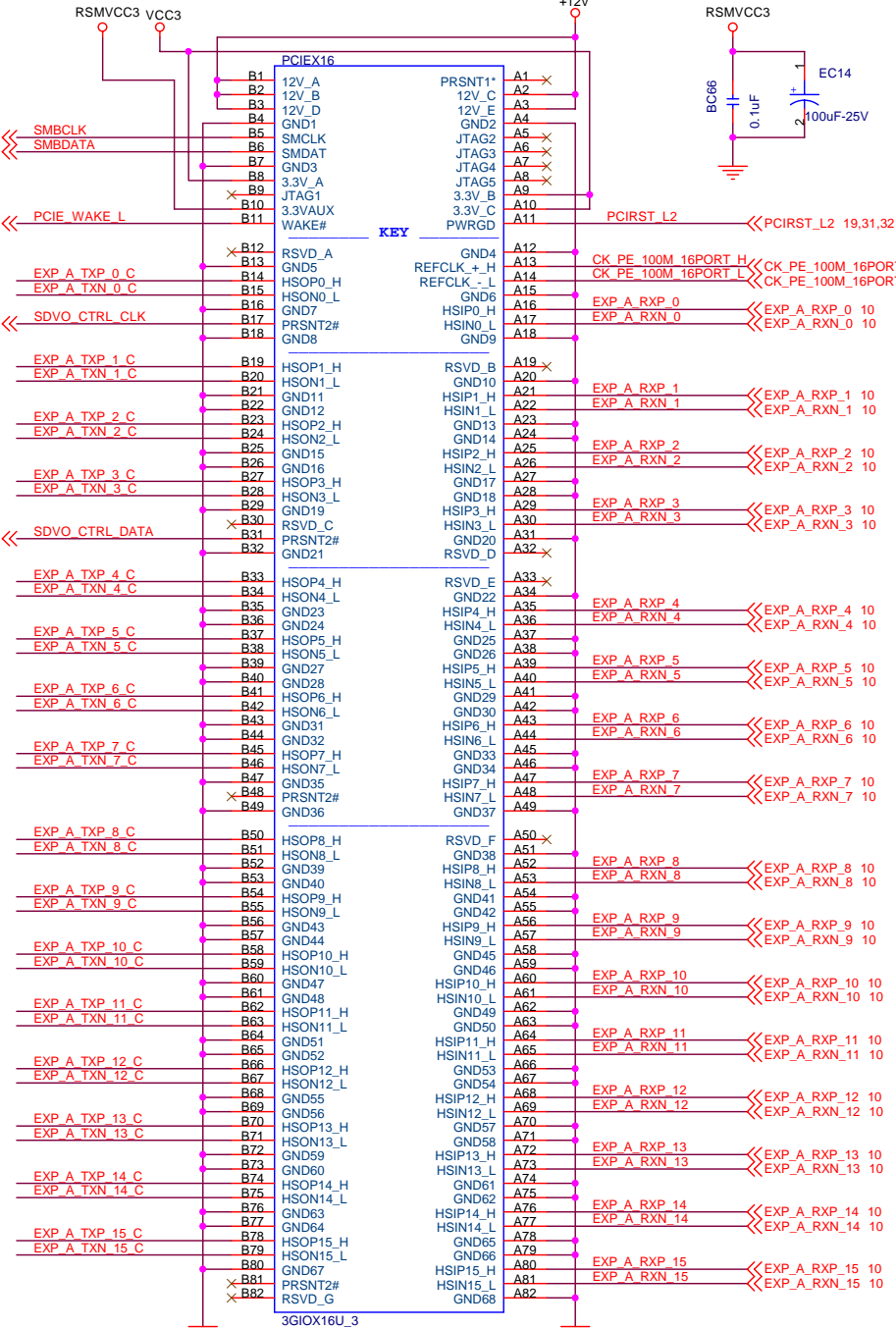


31,32 SMBCLK
31,32 SMBDATA

17 PCIE_WAKE_L

10 SDVO_CTRL_CLK

10 SDVO_CTRL_DATA

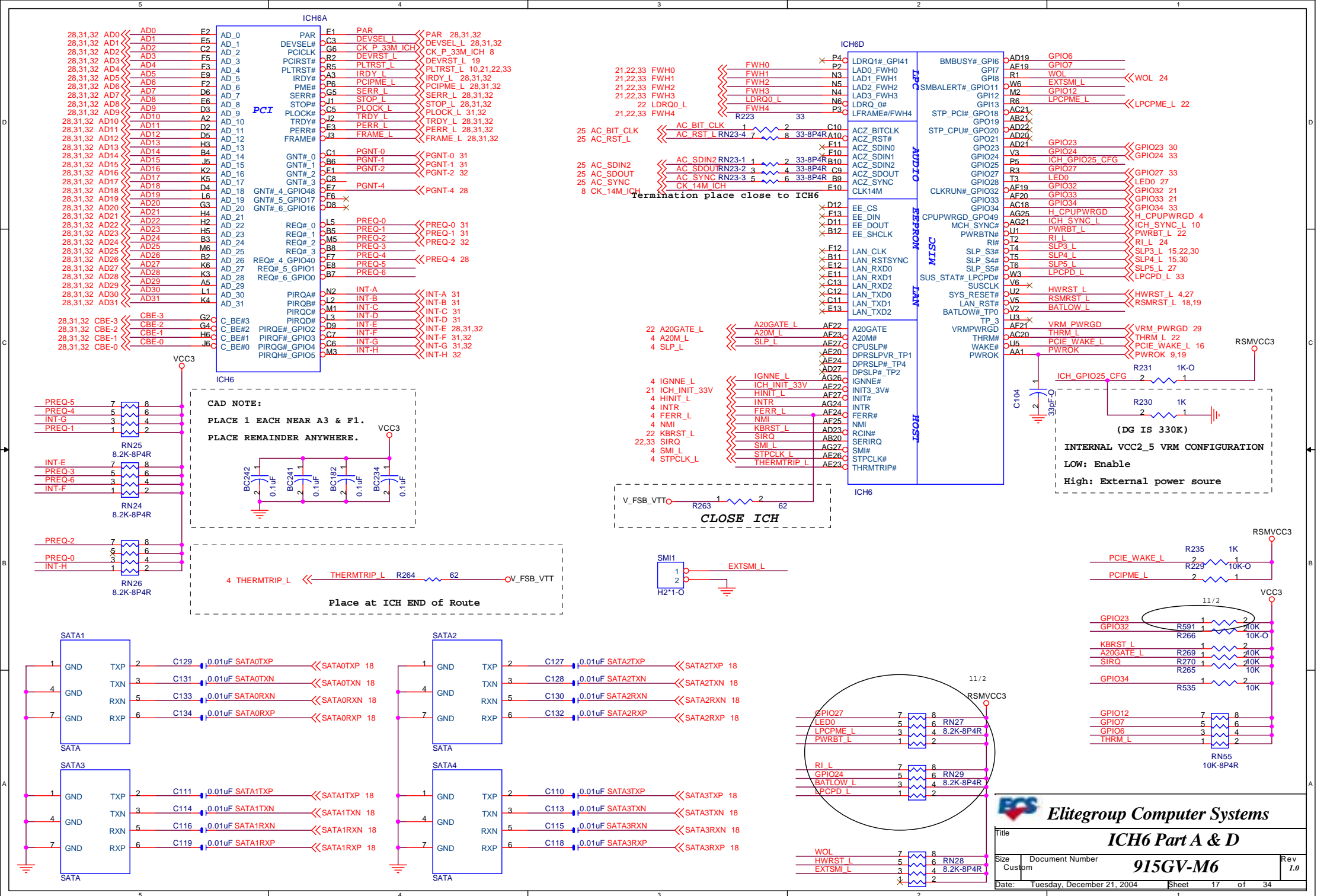


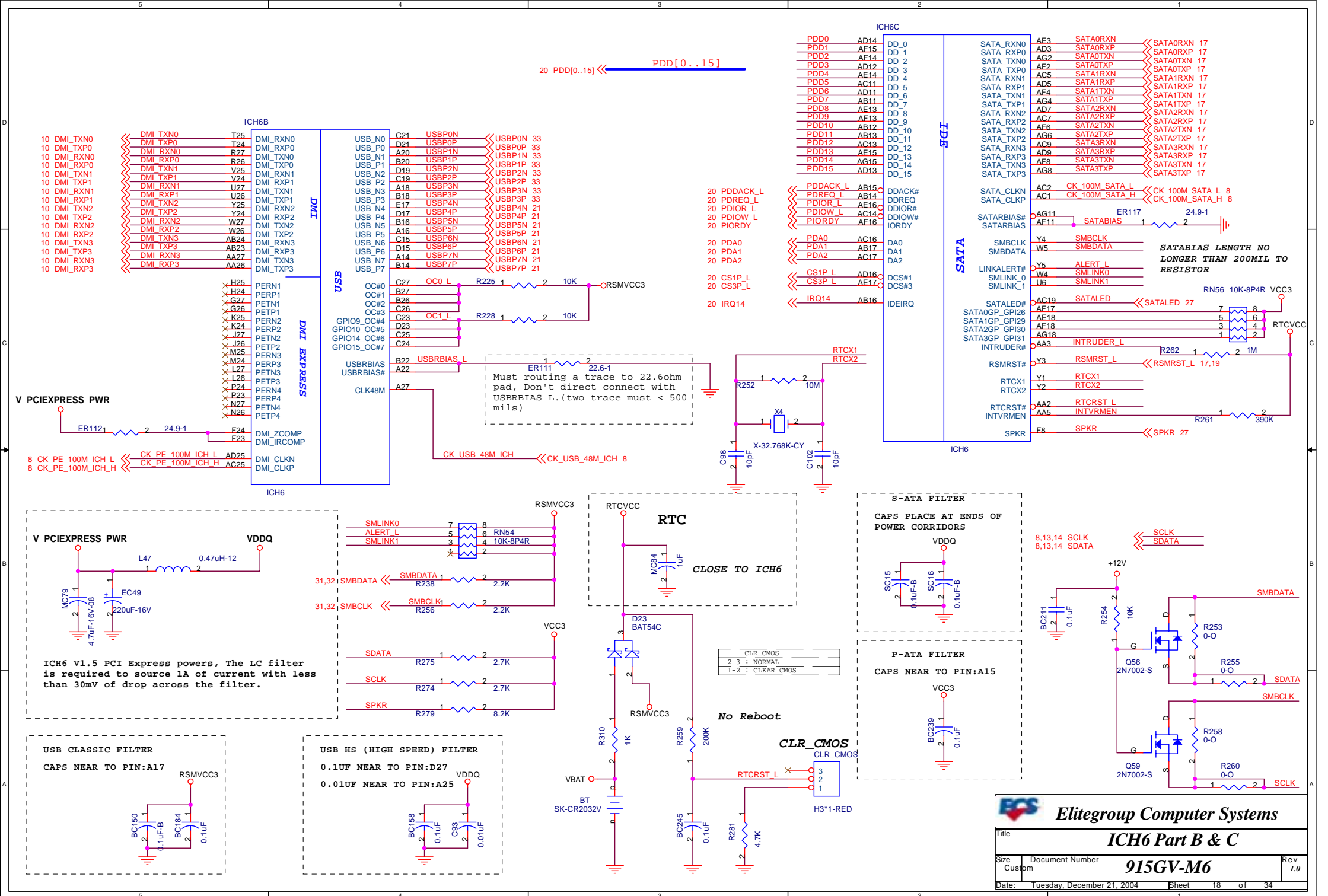
Elitegroup Computer Systems

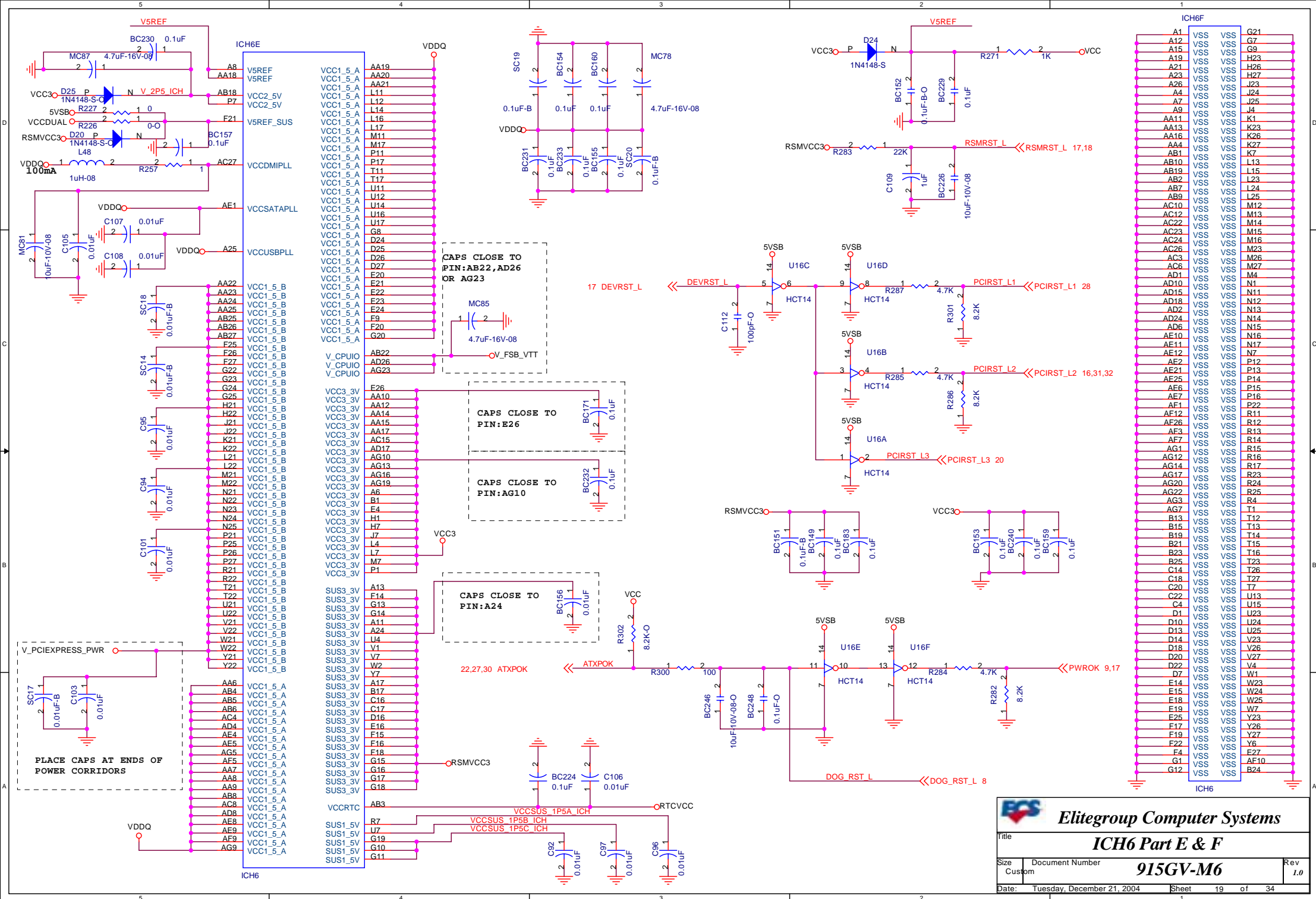
Title: **PCIE 16-PORT**

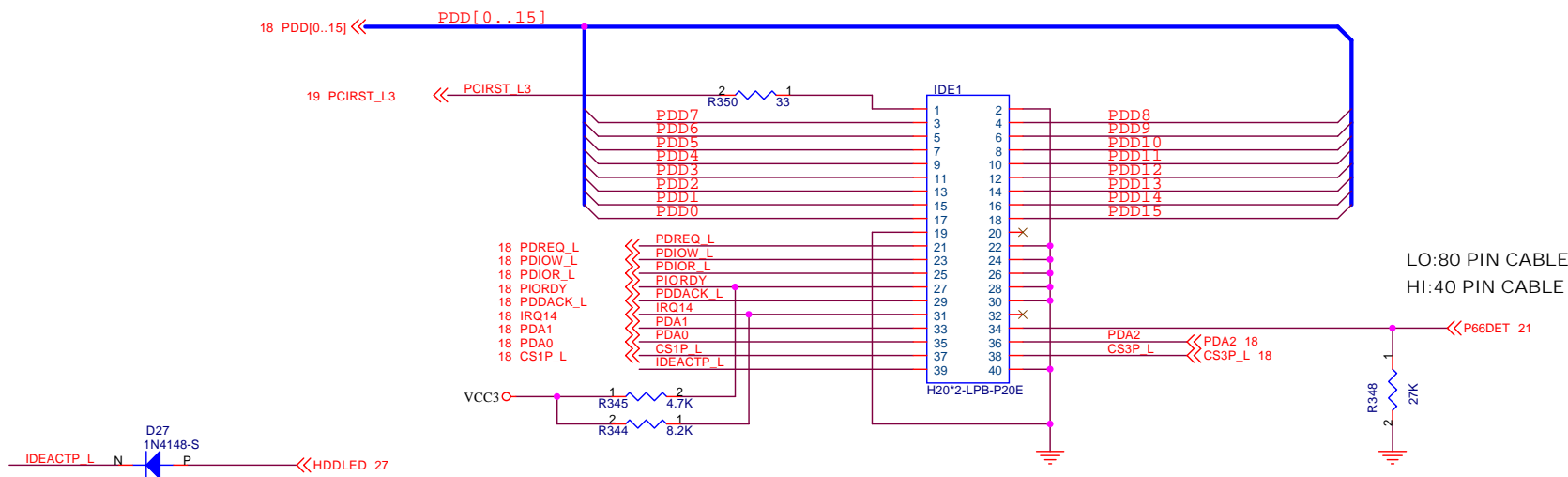
Size: B Document Number: **915GV-M6** Rev: 1.0

Date: Tuesday, December 21, 2004 Sheet: 16 of 34





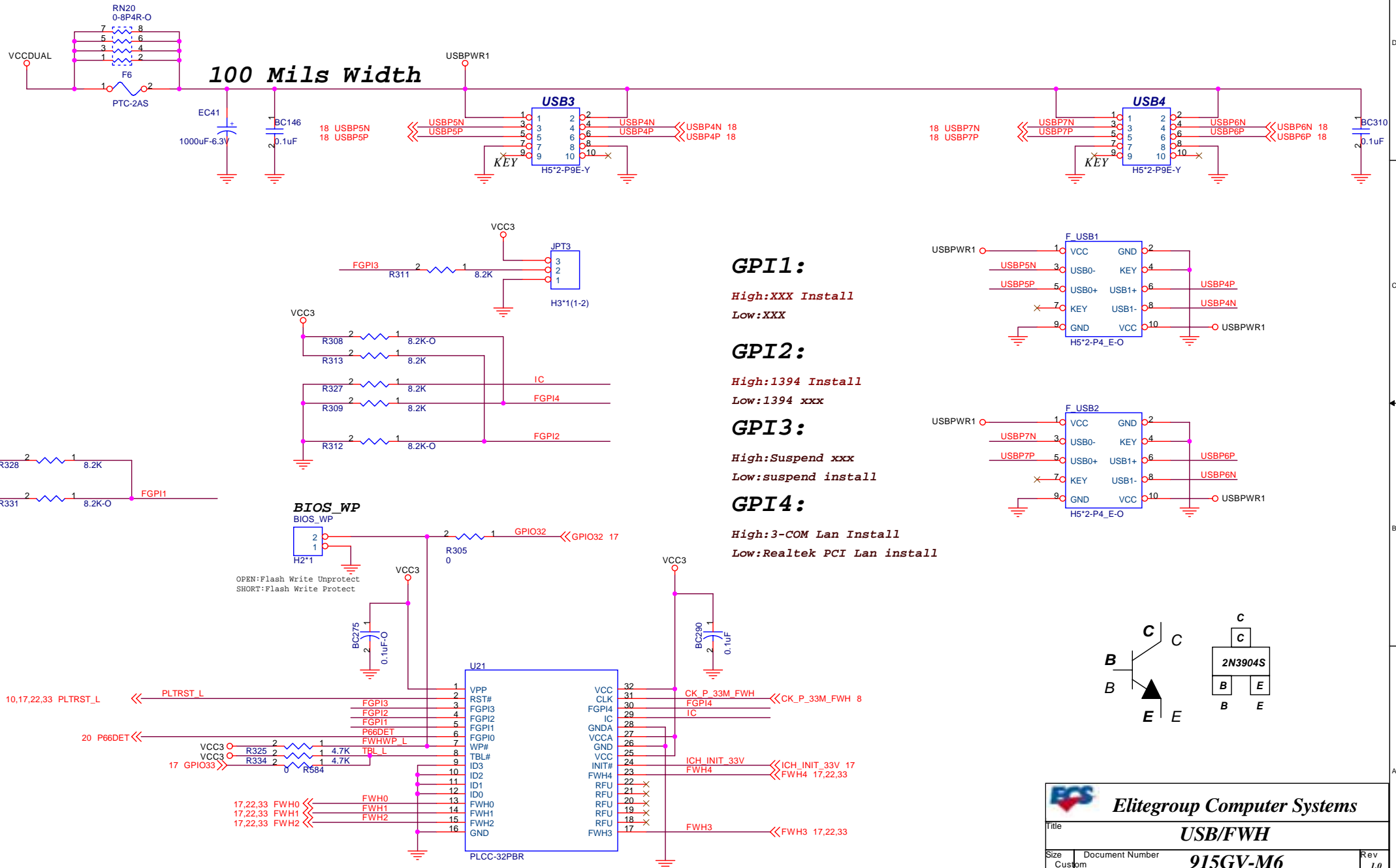


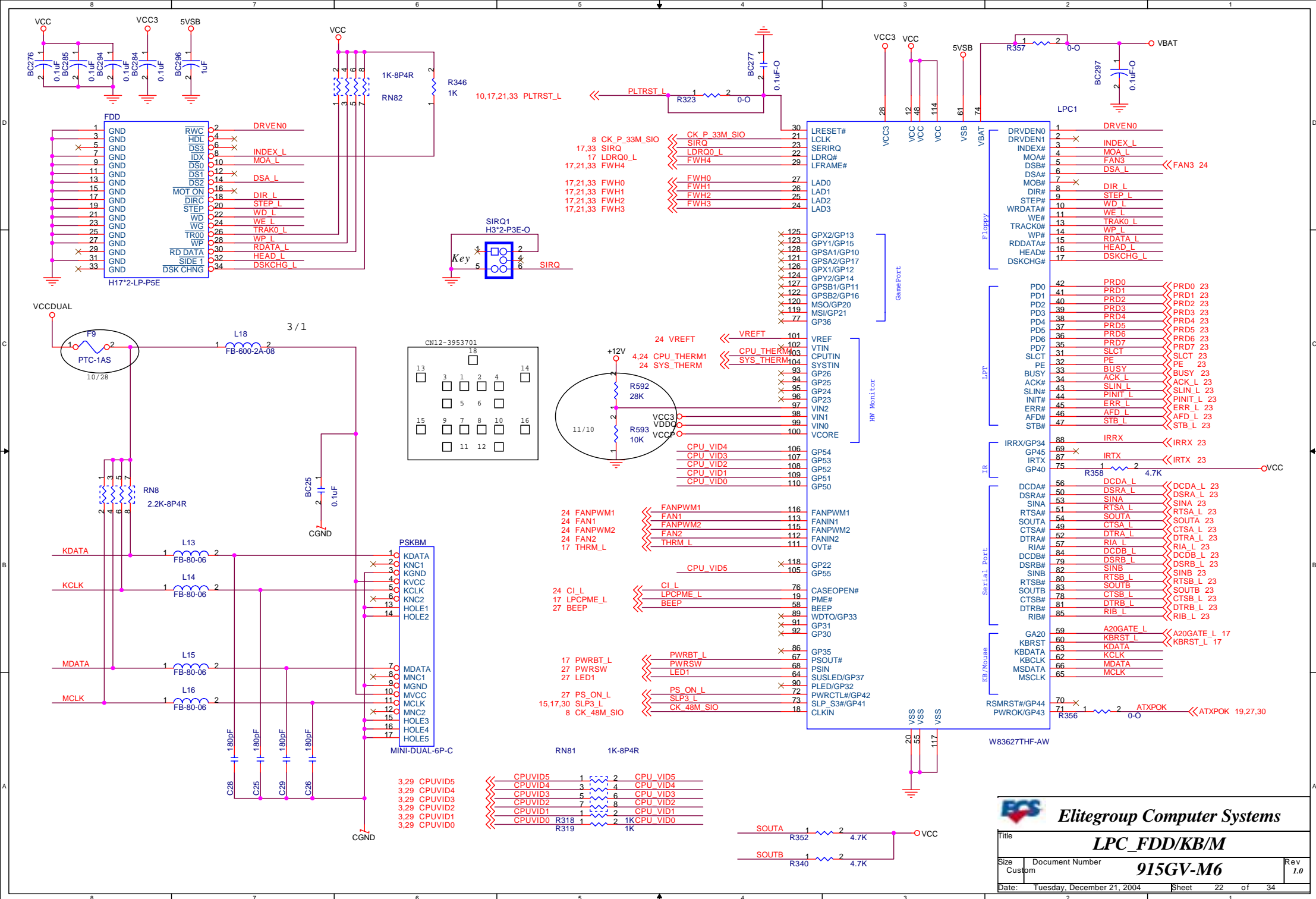


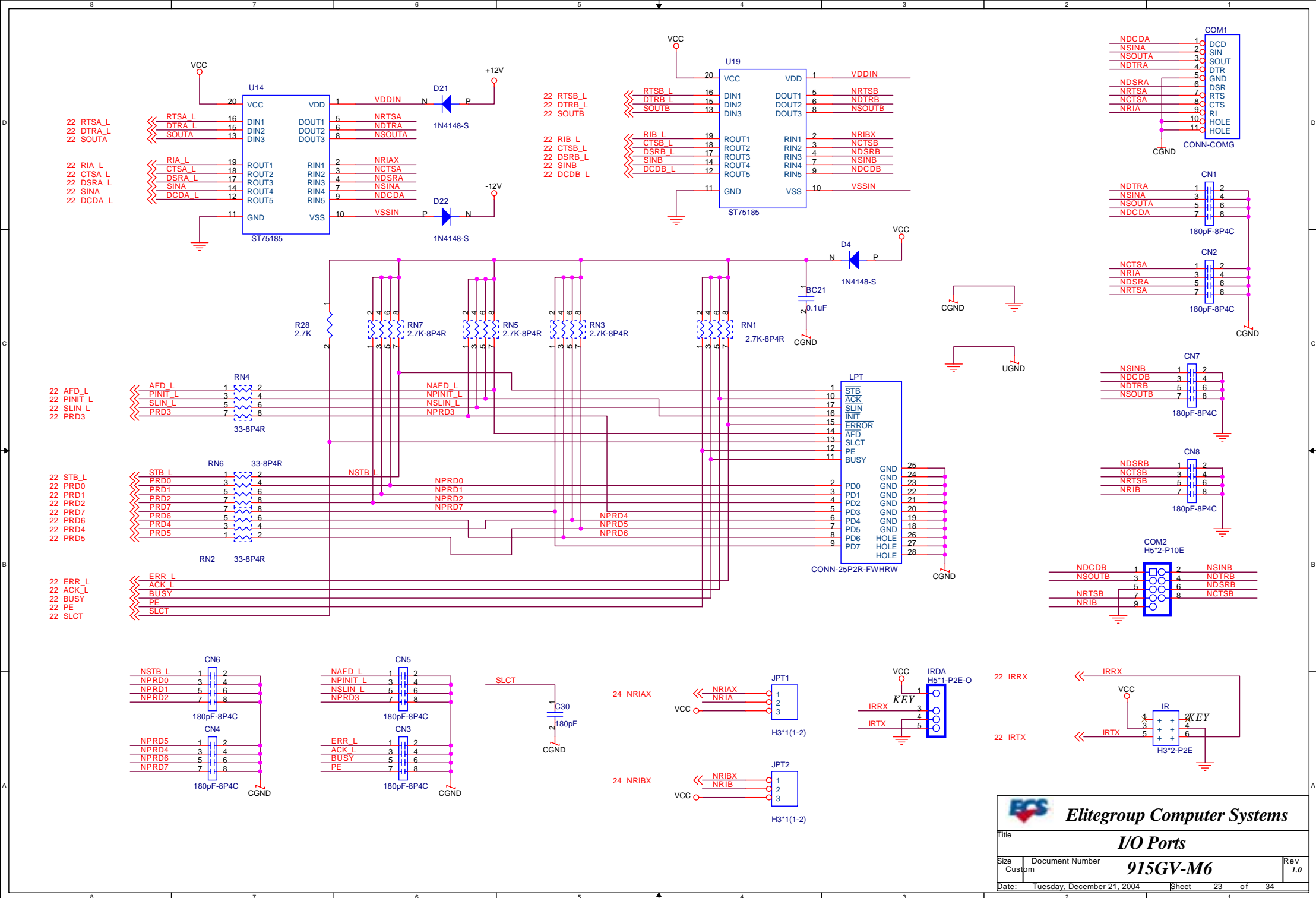
MAX TRACE LENGTH IS 8"

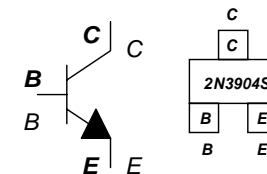
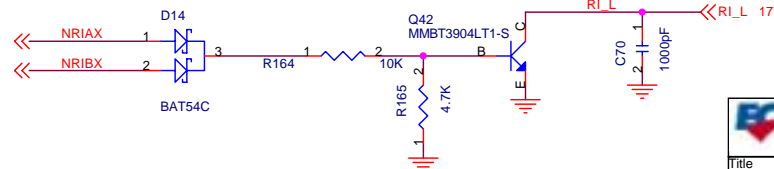
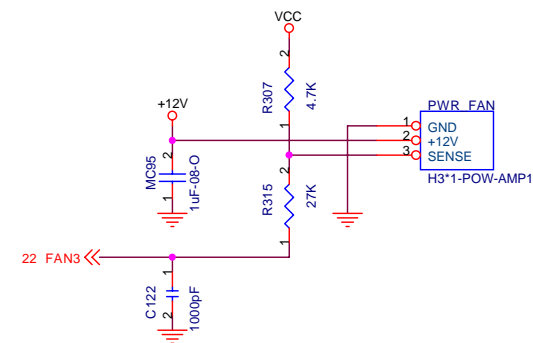
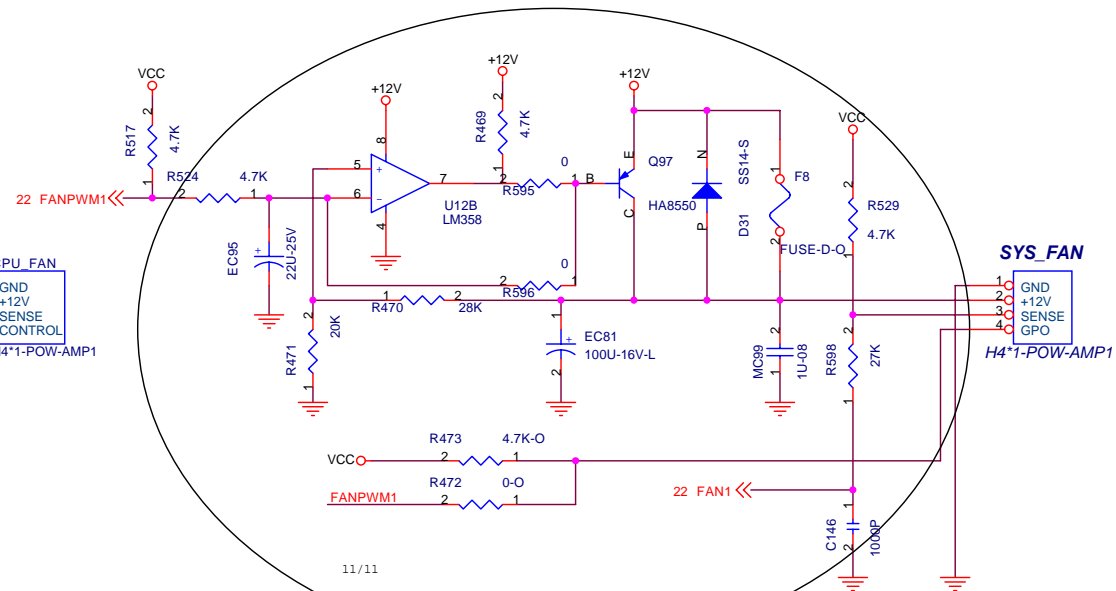
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L, XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.

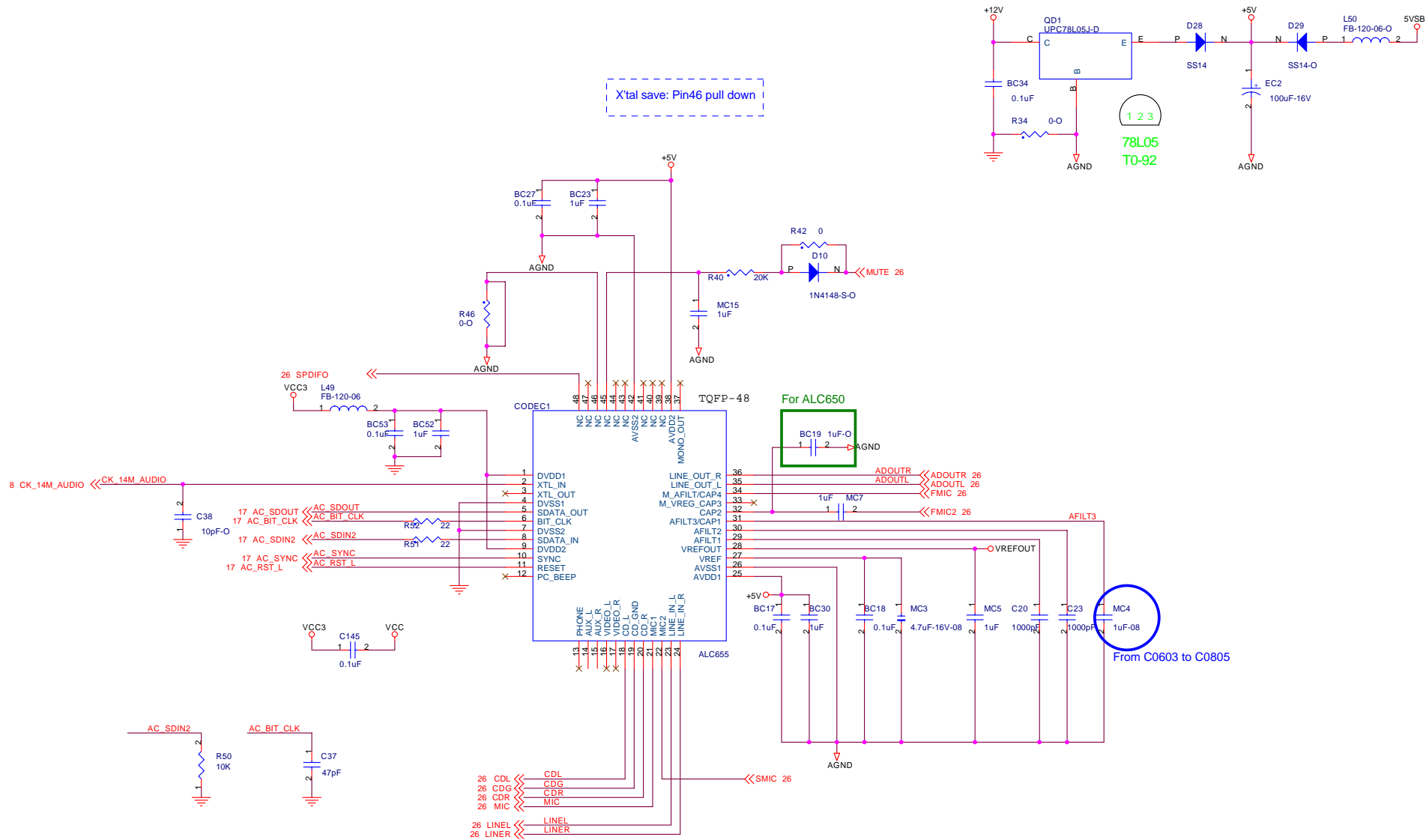
USB PORT INTERFACE



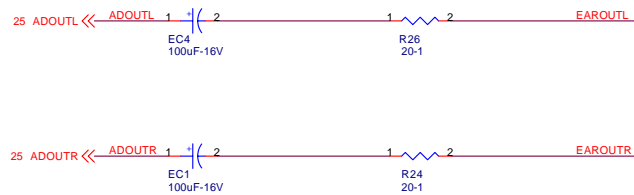




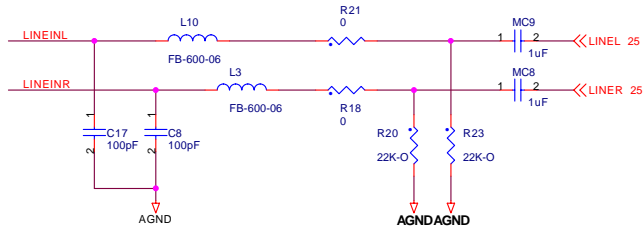




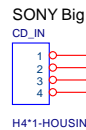
SPEAKER-OUT



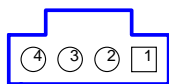
LINE-IN



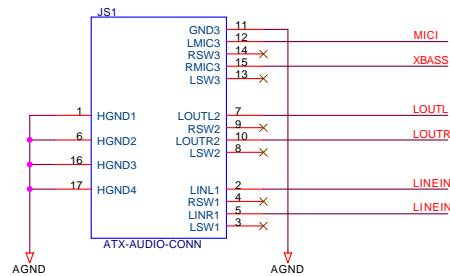
CD-IN



H4*1-HOUSING

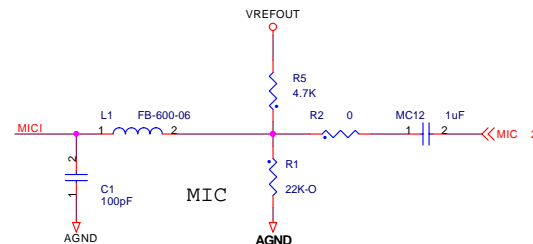
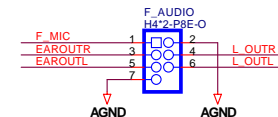
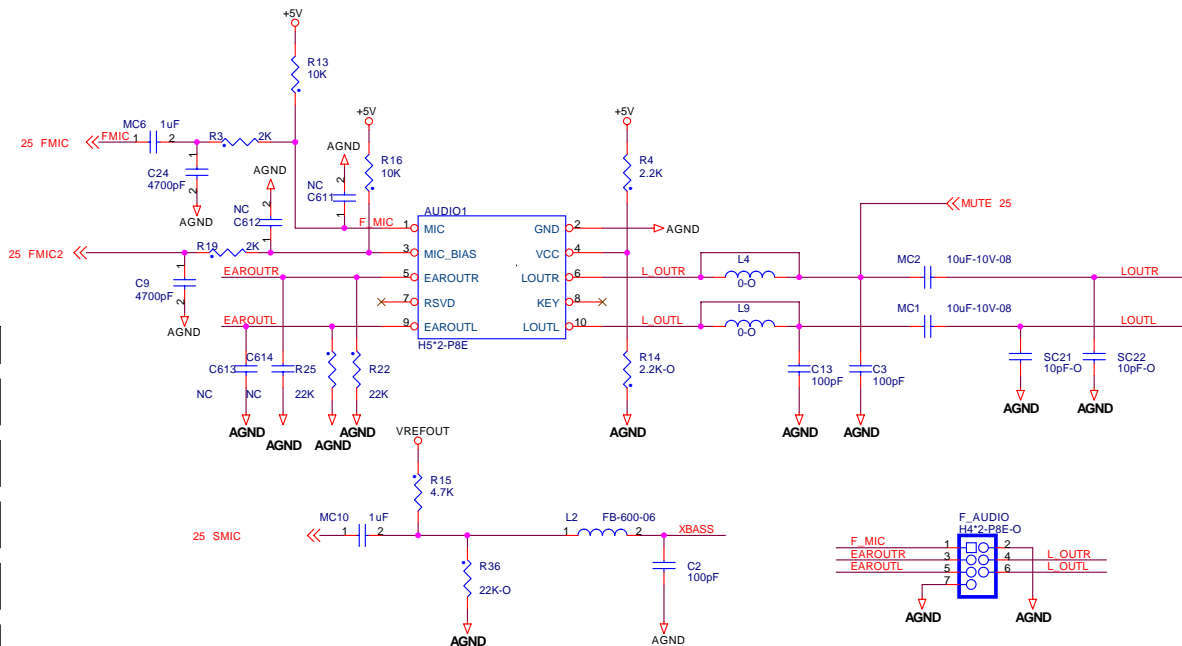
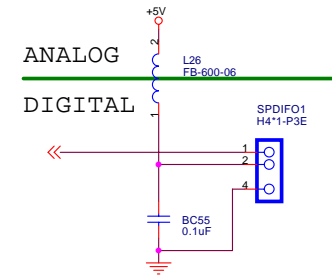


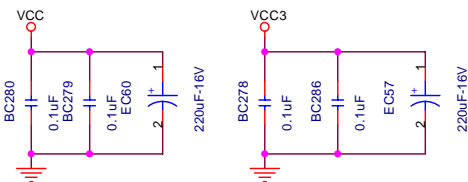
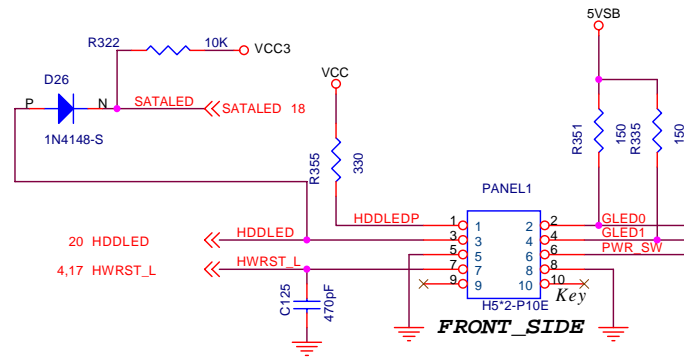
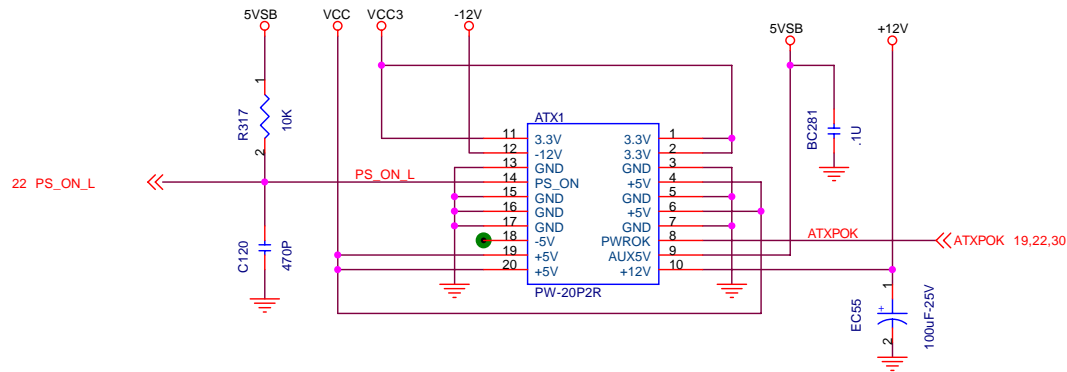
R G G L



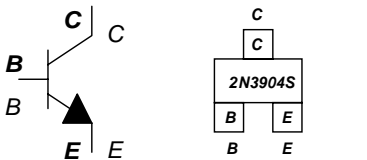
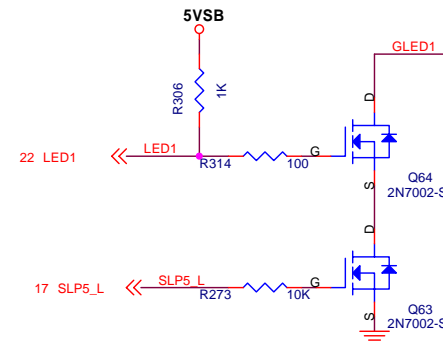
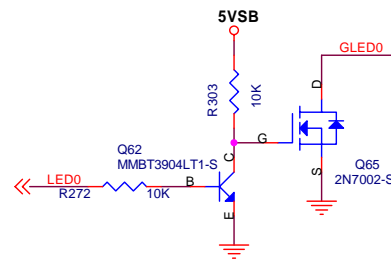
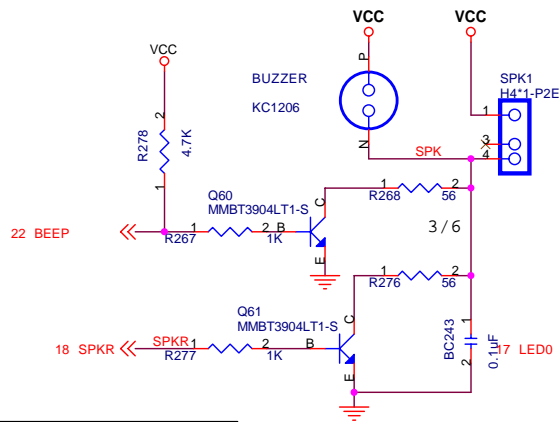
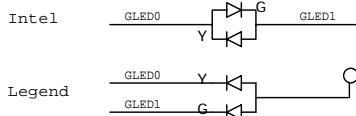
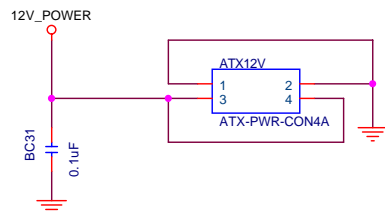
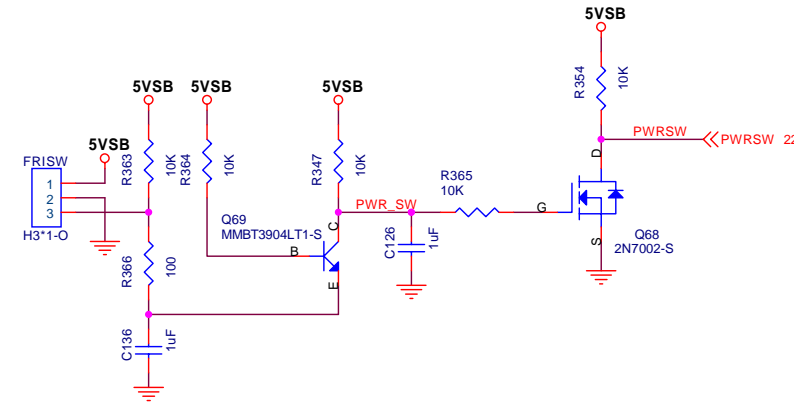
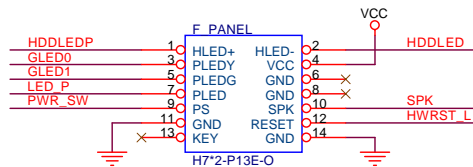
ANALOG
DIGITAL

25 SPDIFO

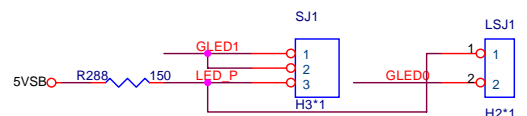




PWR CONN CAPS



	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking	Dark
LSJ1(1,2)	Dark	Dark	Light	Dark
SJ1(1,3)(2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH

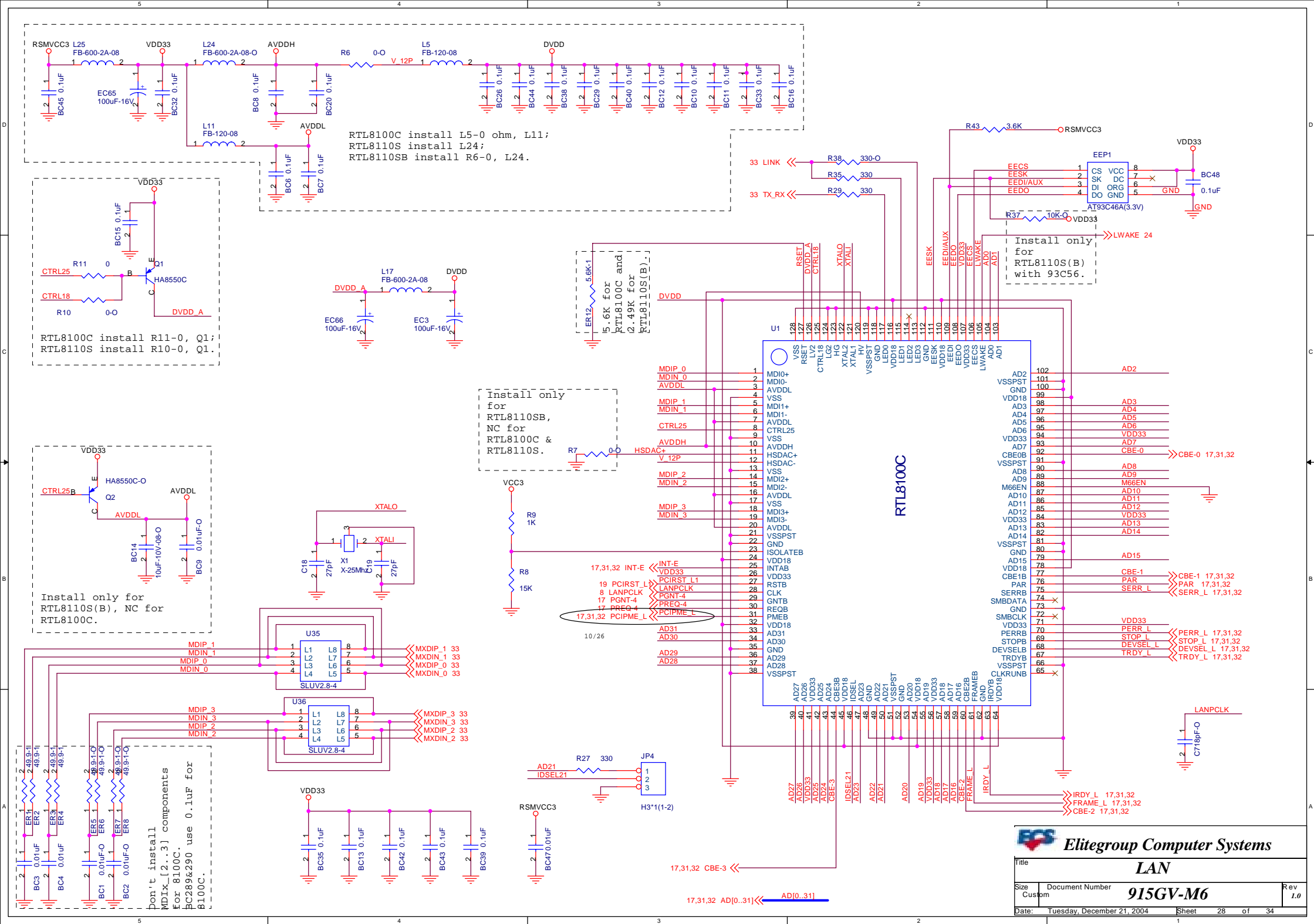


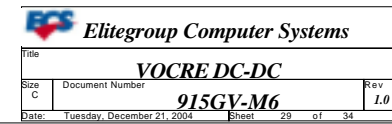
Elitegroup Computer Systems

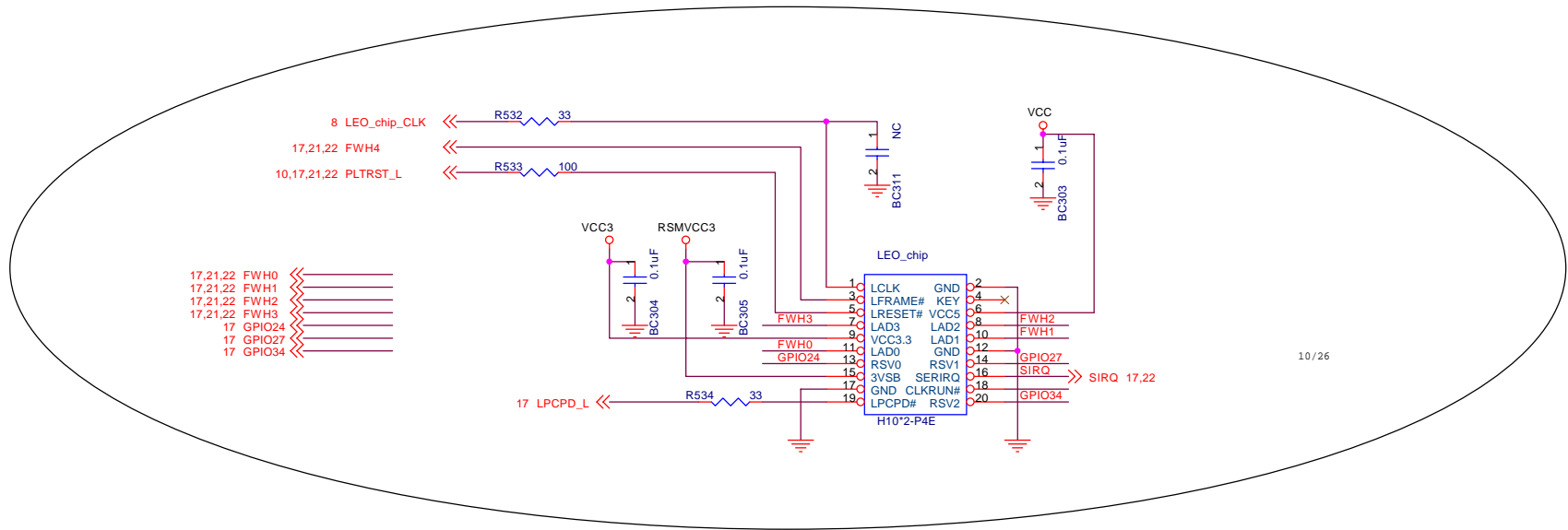
ATX Power & Front Panel

Size B Document Number **915GV-M6** Rev 1.0

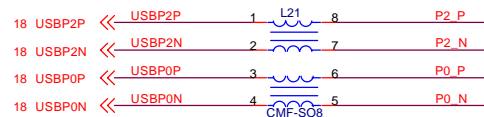
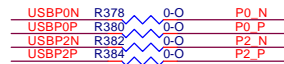
Date: Tuesday, December 21, 2004 Sheet 27 of 34



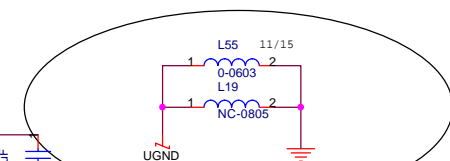
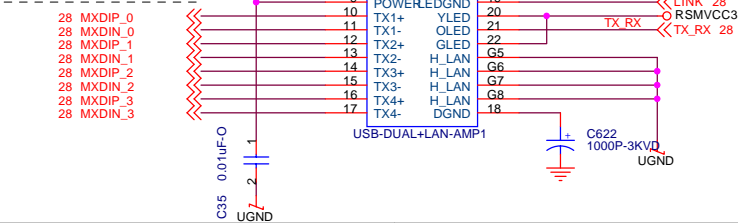
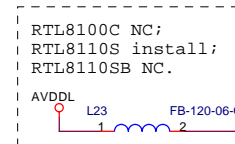
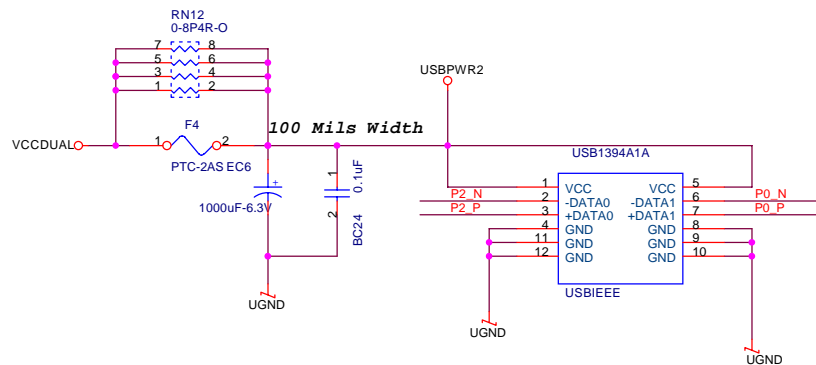
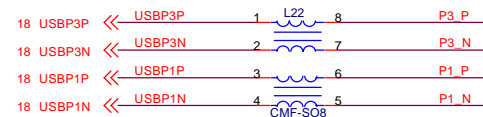
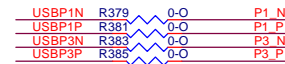




REAR_SIDE



REAR_SIDE



Revision A to Revision B

- 1. R105 & R106 change from Open to 0 ohm 0603, C85 change from Open to 0.01uF 0603, ER89 change from Open to 47 ohm 0603 for system can not boot issue.
- 2. RN21 change from 0 ohm 8P4R to Open, RN22 change from Open to 0 ohm 8P4R for system can not boot issue.
- 3. Add R362 1K ohm 0603 for 2.5V power control issue.
- 4. Add SMI1 header for Legend specifications.
- 5. Add F_USB1 and F_USB2 header for Legend specifications.
- 6. Add I2C header for Legend specifications.
- 7. Add SIRQ1 header for Legend specifications.
- 8. Add JPT2 and JPT3 header for Legend specifications.
- 9. Add IRDA header for Legend specifications.
- 10. Change SYSFAN header for Legend specifications.
- 11. Add CDIN2 header for Legend specifications.
- 12. Add F_AUDIO header for Legend specifications.
- 13. Add F_PANEL and PSW1 header for Legend specifications.
- 14. Add JP3 and JP4 header for Legend specifications.
- 15. Remove PCIe1 and CNR slots and replace with PCI3 for Legend specifications.
- 16. Add F_1394 header and V-port capacitors C137~C144 for Legend specifications.
- 17. R10, R17, Q1 change to Open, ER16 change to 1.3K-1% ohm 0603 for giga lan fail issue.
- 18. R86 change to 270K ohm 0603, C57 change to 1000pF 0603 & C40 change to 5600pF 0603 for VCCP PWM gate jittering issue.
- 19. EC2 & EC3 change to 6mm for PCI card installation mechanical issue.

Revision B to Revision 1.0

- 1. EC25 & EC26 change from 470uF 25V to 1000uF 6.3V, EC35 & EC40 change from 1000uF 6.3V to 1800uF 6.3V for 3DMark 2003 hang issue.
- 2. EC46 & EC47 change from 1000uF 6.3V to 1800uF 6.3V for S3/S4 can not burn in issue.
- 3. Add ER126 24K ohm 0603, delete R194, R197, BC134, R188, ER79, C84, ER78, C82, C83, Change ER77 from 7.5K to Open, D17 from 1N4148 to Open, R190 from 10 ohm 0805 to open, D19 from Open to 1N4148 and R191 from Open to 10 ohm 0805 for RT9214 support.
- 4. Change common mode choke RN9, RN10, RN11 AND RN19 to single R370 ~ R385 for SMT issue.
- 5. Add D28, D29 and L50 for power off audio CD play support.